Feature Article

IEDM 2004: Postmortem

Who presented the most papers at IEDM 2004? How productive were other companies, research and academic institutions?

To answer this question, following rules were applied. Only those sessions relevant to the mainstream IC industry were included in this tally. This means out of total 42 sessions and a late news session, 13 sessions were excluded from the tally. For each paper, one point was given to the lead author company or institution and a half point was given to each co-author company or institution.

Now the tally is in.
Samsung tops the list with 21.5 point, easily surpassing number two IBM, which scored 16.5 points. Samsung's score came from 21 papers of its own and one jointly authored paper with IBM. STMicro and Toshiba take the next two spots with 12 and 11 points, respectively. Intel, the largest IC manufacturer, is ranked 5th with a score of 8.

So, what's the correlation between the revenue and the productivity at the IEDM? Or is there a correlation? The table below shows a list of 2004 top-10 semiconductor manufacturers based on IC Insights 2004 revenue projection and the number of papers they presented at IEDM 2004.

1. Intel	8
2. Samsung	21.5
3. TI	3
4. Renesas	3
5. Infineon	7.5
6. Toshiba	11
7. STMicro	12
8. TSMC	4.5
9. NEC	5.5
10.Freescale	4.5

IBM is missing in the above table because its Microelectronics division is not ranked among the top-10 merchant semiconductor manufacturers. Between the 11th and 20th rankings, Philips (ranked 11 th) got 11, Fujitsu had 5 and Sony scored 2.5. Other notables: AMD/Spansion got 0.5, Hynix also scored 0.5. Micron did not score. Overall, there does not seem to be much correlation between the revenue and productivity at IEDM. However, you can tell which companies take it more seriosuly to present research results in conferences such as IEDM.

Among research and academic institutions, European research institutions were most productive with CEA-LETI and IMEC leading the chart with scores of 7.5 and 7 respectively (see chart below.) A strong performance by National University of Singapore earned them a score of 6, an indication of government support and emphasis on semiconductor research in this Southeast Asian city state. See below for a score chart (in random order) for selected research and academic institutions.

CEA-LETI (France)	7.5
IMEC (Belgium)	7
ISMT (US)	2
ASET (Japan)	3
AIST (Japan)	2
Selete (Japan)	4
National University of Singapore	6

Stanford University	4.5
University of California, Berkeley	3
University of Texas, Austin	5
Purdue University	3.5
National Chia Tung University	4.5

The overall top-10 list for the number of papers presented at IEDM 2004 looks like this.

1. Samsung	21.5
2. IBM	16.5
3. STMicro	12
4. Toshiba	11
5. Intel	8
6. Infineon	7.5
6. CEA-LETI	7.5
8. IMEC	7
9. National University of Singapore	6
10.NEC	5.5

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IEDM 2004 celebrates 50th anniversary.
STOL, Nov. 2004

This year marks the 50th anniversary of International Electron Devices Meeting (IEDM). To celebrate 50th anniversary, IEDM features special events when it holds an annual meeting from Dec. 13 to 15 in San Francisco. Conference attendees will receive a DVD containing the technical digest contents for the past 50 years. There will be a special reception and historic-paper poster exhibit on Monday evening. On Dec. 14, Dr. Richard E. Smalley, Rice University Professor and 1996 Nobel laureate in Chemistry will speak at the IEDM Tuesday Luncheon.

During the past 50 years IEDM has served as a premier forum for the semiconductor technology innovation. 1950's was the dawn of the solid state electronics after the invention of transistor in 1948 by Bardeen, Brattain and Shockley at Bell Labs. The invention of the integrated circuits in 1958 by Jack Kilby at TI ushered in an era of the integrated circuits in 1960's that has since revolutionized the electronics industry. 1970's brought in the proliferation of MOS technology. As a result of continued innovation in MOS technology, integrated circuits evolved since 1980's from LSI to VLSI to USLI.
As IEDM celebrates 50 th anniversary this year, we are at a critical juncture in silicon technology innovation. It used to be that the scaling of MOS technology increased circuit density and device performance simultaneously. Every 18 months or so, the number of transistors in a single chip increased by two-folds along with improved transistor switching speed – commonly known as Moore's law.

Not any more though, or at least it has become difficult to achieve performance improvement as MOS devices approach scaling limits. Strained silicon and high k gate dielectric are the hottest agenda today to overcome this difficulty. Strained silicon research is yielding good results and are being implemented in manufacturing process. High k dielectric is still a work in progress. Development of manufacturing-worthy high k dielectric has not been easy as it deals with heart and soul of MOS transistor - gate dielectric. In fact, the whole gate stack needs to be re-engineered in conjunction with high k dielectric development.

IEDM 2004 program reflects these current technological challenges. Two sessions have been set up for strained silicon and also for high k. In addition, there's a one session dedicated to metal gate engineering. Flash memory technology, another hot item in recent years, also gets two sessions.

For short summaries of each paper, visit IEDM home page at www.ieee.org/conference/iedm.

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Intel and IBM vie for supremacy in logic technology.
STOL, Nov. 2004

For generations, Intel's logic technology outperformed the rest of the industry. Thanks to aggressive transistor scaling and well-engineered device architecture, MOS transistor drive currents from Intel are the industry's best at 130nm and 90nm nodes. Intel's transistor performance is what powers its microprocessors running at the record-setting clock frequencies. SRAM cell size and backend interconnect design rules of Intel are among the most competitive.

Although Intel's logic performance remains the envy of many other companies, it is losing the competitive edge it used to have. Intel is still the leader in bulk CMOS logic technology. However, because of the emergence of SOI logic technology in the high-performance logic arena, Intel can no longer claim performance leadership at 130nm and 90nm nodes.

IBM has the platform logic technology based on bulk CMOS and the high-performance logic technology based on SOI CMOS. The performance of IBM bulk CMOS logic technology lags Intel's. However, the performance of IBM high-performance SOI logic technology is excellent at 130nm and 90nm nodes with speed performance eclipsing Intel's.

Given below is a comparison of logic technology performance for the two companies at 130nm and 90nm nodes, based on published data at IEDM from 2001 through 2003.

130nm node in 2001:

The MOS transistor drive currents of Intel, reported at IEDM 2001, are 1300µA/µm for N-ch and 660µA/µm for P-ch at Vdd=1.4V with off-state leakage current of 100nA/µm. At the same conference, IBM reported transistor drive currents of 1240µA/µm for N-ch and 660µA/µm for P-ch for its SOI MOSFET's. The IBM drive currents are the values without self-heating projected at the same measurement condition as Intel.

Inverter stage delay of Intel is 6ps at Vdd=1.4V with Ioff=10nA/µm while IBM reported an inverter stage delay of 5.46ps at Vdd=1.2V. IBM claims its stage delay is the fastest at 130nm node. Although that claim could be true, it cannot be verified independently because IBM did not provide the off-stage leakage for the stage delay quoted in the paper.

SRAM cell size is 2µm**2 for Intel and 1.8µm**2 for IBM. The smaller SRAM cell of IBM is made possible partly due to tighter design rules allowed in SOI technology.

90nm node as of 2002:

At 90nm node, Intel logic performance is again facing a challenge from IBM. At IEDM 2002, Intel and IBM each presented a paper on 90nm logic technology; Intel using bulk CMOS and IBM using SOI CMOS.

Transistor drive currents of Intel 90nm technology are 1260µA/µm for N-ch and 630µA/um for P-ch at Vdd=1.2V with off-state leakage of 40nA/µm. MOSFET gate length is 0.5um. These drive currents are impressive and were achieved using strained-silicon channel MOSFTET. However, inverter stage delay was missing in the Intel IEDM 2002 paper, indicating the technology was not mature enough at the

time.

Drive currents of IBM SOI transistors, reported at the same conference, were 1322uA/um and 599uA/um at Vdd=1.2V for N-ch and P-ch, respectively. These are the projected values at the off-state leakage currents of 70nA/um for N-ch and 80nA/um for P-ch without self-heating. MOSFET gate length was 0.46um and strained-silicon channel was not used in IBM transistors. IBM N-ch drive current is 5% higher than Intel but P-ch drive current is 5% lower with higher leakage currents for IBM. So, Intel has a slightly edge in MOSFET DC performance.

However, IBM SOI transistors shine in AC performance. While Intel did not provide inverter stage delay at IEDM 2002, inverter stage delay of IBM is 5ps at Vdd=1.2V, the fastest speed reported at 90nm node. This excellent stage delay is a result of high drive currents and low junction capacitances of SOI transistors.

90nm node as of 2003: Intel's shift in 90nm transistor strategy:

One year after its first 90nm technology presentation at IEDM 2002, Intel disclosed its manufacturing-ready 90nm logic technology at IEDM2003. For the manufacturing-ready 90nm technology, Intel abandoned strained-silicon channel MOSFET using epitaxial SiGe layer, which was the highlight of its 2002 paper. Instead, it opted for a less aggressive and manufacturing-friendly approach to implementing strained-silicon for the volume-manufacturing version.

With the new strained-silicon implementation approach, Intel P-ch drive current in 2003 was improved to an incredible 700μA/μm from 630μA/μm a year before. This P-ch drive current is by far the best at 90nm node and superior to IBM. N-ch drive current remained the same at 1260μA/μm as 2002 but N-ch gate length was scaled down from 0.50μm in 2002 to 0.45um in 2003.

Transistor drive currents of Intel in 2003 indeed look excellent. As Intel stated in the 2003 paper, this is the first time that strained-silicon transistors are implemented in a manufacturing technology, which in itself is a significant milestone in the evolution of CMOS technology.

However, inverter stage delay is again missing in Intel's 2003 presentation, indicating Intel still had some work left to integrate these superb N-ch and P-ch transistors into a single CMOS process.

Because of the unavailability of inverter stage delay data from Intel, the logic technology speed title at 90nm node should go to IBM.

The SRAM cell sizes of Intel and IBM are very close; 1μm**2 for Intel and 0.992μm**2 for IBM. Intel has done a good job to realize bulk CMOS SRAM cell with 1um**2 size. On the other hand, IBM SRAM cell size is not a standout, considering it is an SOI technology. However, IBM SRAM cell, "thin cell" as it is called by IBM, offers a good manufacturing margin at all critical layers. In particular, poly gates in the IBM SRAM cell are laid out in the same orientation, making poly gate CD control easier with a wider process window.

Summary:

Based on speed performance and SRAM features, STOL believes IBM SOI logic technology is a winner over Intel bulk CMOS logic technology at 130nm and 90nm. In some areas of comparison, the difference was not significant. In other areas, the comparison could not be made conclusively because of the lack of data. Nonetheless, published data was sufficient to conclude IBM over Intel in logic performance comparison.

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